ANALYSIS OF TIME-DOMAIN PRE-EMPHASIS METHOD FOR HIGH-SPEED VLSI SYSTEMS

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Abstract: The perspective digital pre-emphasis technique based on a pulse-width modulation (PWM) is introduced. The transmitter pre-emphasis (equalization) is commonly based on an FIR (Finite Impulse Response) filter. The PWM pre-emphasis uses a timing resolution instead of an amplitude resolution to adjust the filter transfer function. This fits well for the future ultra low voltage high-speed CMOS systems.

Keywords: time-domain, pre-emphasis, high-speed, PCB, interconnect, signal integrity

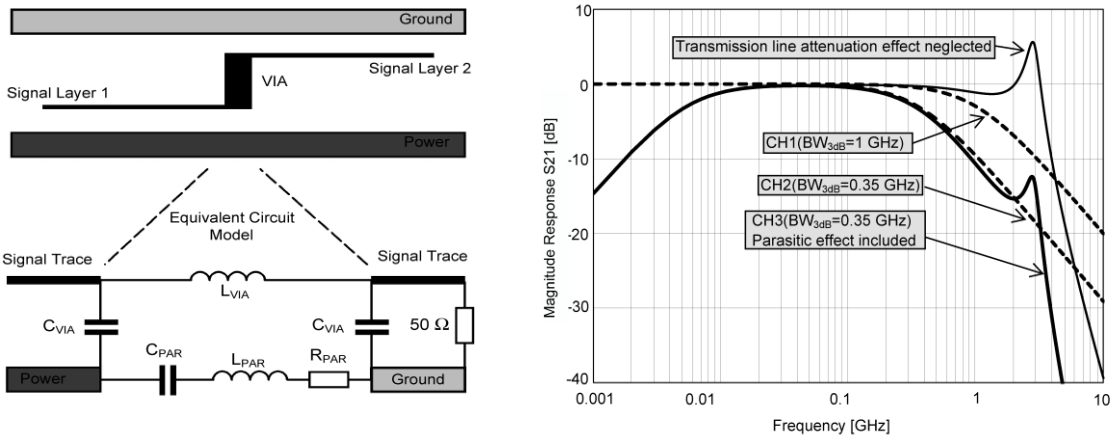
1. INTRODUCTION

In this paper, we describe the application of PWM pre-emphasis to the equalization of higher-order printed circuit boards (PCBs) backplane channels. It provides an alternative to FIR pre-emphasis with advantages in the light of developments in CMOS scaling. In section 2 of this paper the channel properties and principle of PWM pre-emphasis method is described. Two transmitter equalization methods, conventional FIR and presented PWM, are analytically compared. Finally, frequency domain comparison of both pre-emphasis methods for a higher-order channel is shown. An advanced model of transmission lines developed on the basis of practical measurements in MathCAD environment is used. We show that the 1st-order PWM pre-emphasis is able to compensate higher-order channel without increasing the number of taps much better than the conventional FIR method.

2. PULSE-WIDTH MODULATION PRE-EMPHASIS

2.1. CHANNEL PROPERTIES

In this case, the signal conductor is routed through a single power or ground plane such that both sides of this plane are used as the signal reference planes throughout the signal propagation path. Fig. 1a depicts this situation, in which the signal current jumps from the topside of a ground plane through the bottom side of the same ground plane by using an electrical via. The reference plane could also be a power plane. Due to two different reference planes being used on the return path, an impedance discontinuity arises at the location of the electrical via. This impedance discontinuity is due to the capacitance between the power and ground planes that is intended to be part of the return path. At the location of the via, a displacement current component will allow the return current to follow alongside the via until it encounters the power plane, in which the power plane then carries the return current alongside the signal current. In addition to the local capacitive impedance discontinuity occurring from the capacitor that is connected between the power and ground planes at the location of the via, parasitic capacitances also occur between the via and the two reference planes (C_{VIA}). Together, these impedances can be incorporated into an equivalent circuit model also shown in Fig. 1a. In this model, the impedance discontinuity between the power and ground planes is modeled as a series *R-L-C* circuit, in which C_{PAR} is the local capacitance, L_{PAR} is the parasitic inductance associated with the capacitance, and R_{PAR} is the parasitic resistance of the capacitor.



a) b)

Fig. 1. a) Equivalent circuit model for transmission channel with higher-order transfer function b) Two theoretical channel responses for different BW_{3dB} setting and analyzed higher-order transfer function.

For a 62 mil thick PCB with power and ground planes located on the outer surfaces of the PCB, measurements of the local impedance between these two planes yielded values of C_{PAR} = 300pF, L_{PAR} = 2.8 nH, and R_{PAR} = 0.5 Ω [1], [2]. The parasitic via capacitances were also determined to be 0.1pF. Of course, for smaller separation distances between the power and ground planes, it is expected that C_{PAR} would increase in value, while L_{PAR} and R_{PAR} would both decrease in value. The via inductance was also determined to be 0.4nH. Fig. 1b illustrates our analyzed high-order channel transfer function together with two types of theoretical channels. The typical bandwidth parameter (BW_{3dB}) is equal to BW_{3dB} = 1 GHz in the first case and BW_{3dB} = 0.35 GHz for more lossy channel is the second case. The strategy which is commonly used to minimize the signal degradations at higher frequencies includes a local surface-mountable capacitor between the power and ground planes that is also near to the location of the via. This additional on-board capacitance needs to be properly sized in order to provide the desired reduced signal degradations. This capacitor is also necessary in order to greatly increase the capacitance between the power and ground planes. It is this capacitance that is mostly responsible for the signal degradations on the output signal. Without this precaution overshoot and undershoot are both present on the output signal. The undershoot causes a kind of droop on the flattop portions of the output signal. This droop is undesirable since it can cause degradation in the input noise margin at the output signal. For very small clock risetimes and falltimes (below 100 ps) significantly more high-frequency degradations occur on the output signal, as well as the continuance of the droop on the flattop portions of the output signal. In addition, it is assumed that the load is matched to the transmission line, so that the only discontinuity that should appear on the frequency response is due to the signal jumping between the power and ground planes. However, our practical results show that increasing the capacitance between the power and a ground plane does not eliminate the risetime and falltime stalls, which are highly undesirable. Fig. 1b shows the channel transfer function CH3 without any additional capacitance between the power and ground planes. The bandpass result is highly undesirable since it will cause drooping of the flat-top portion of the input signal to appear on the output signal. The resonance is also highly undesirable since it can cause signal ringing. Both FIR and PWM pre-emphasis techniques are tested on this high-order channel.

2.2. IMPULSE RESPONSES AND POWER SPECTRAL DENSITY ANALYSIS

The transmitter equalization filter is commonly realized as FIR filters [3], [4]. The purpose of this operation is to increase amplitude for the first bit after a logic transition relative to successive bits. The PWM pulse shape is similar to Manchester code for duty-cycle (d) parameter setting to 50 %. A duty-cycle of 100% corresponds to transmission of normal polar NRZ. The pulse definition for $p_{FIR}(t)$ corresponds with FIR pulse (1) and for $p_{PWM}(t)$ defines PWM pulse (2),

$$p_{FIR}(t) = \begin{cases} 0 & t < 0 \\ r & 0 \le t < T_s \\ r-1 & T_s \le t < 2 \cdot T_s \\ 0 & 2 \cdot T_s \le t \end{cases}, \tag{1}$$

where r and r-1 denote the values of the first and the second FIR taps, respectively, and T_s represents the symbol duration (T_s = 200 ps).

$$p_{PWM}(t) = \begin{cases} 0 & t < 0 \\ 1 & 0 \le t < d \cdot T_s \\ -1 & d \cdot T_s \le t < T_s \\ 0 & T_s \le t \end{cases}, \tag{2}$$

where d denotes the duty-cycle ($0.5 < d < 1$ fits best to PCB backplane) and T_s again represent the symbol duration (T_s = 200 ps).

According to the pulse definitions above the impulse responses for both FIR pulse and PWM pulse are calculated over a channel with defined bandwidth (BW_{3dB}), see Fig. 2a. The optimal duty-cycle setting is strongly dependent on channel characteristics as well as r parameter adjustment at FIR pre-emphasis filter, see Fig. 3a. However, it is obvious that the optimal value of both r and d parameters is similar for the same BW_{3dB} setting.

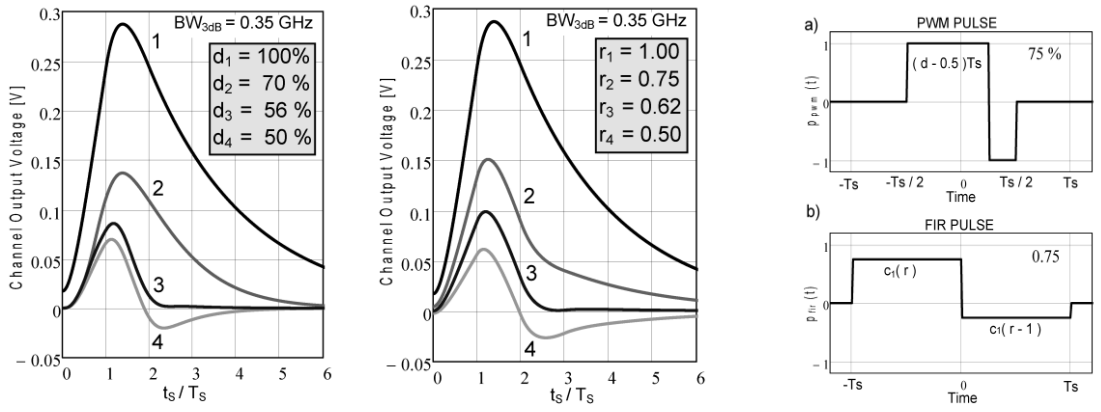


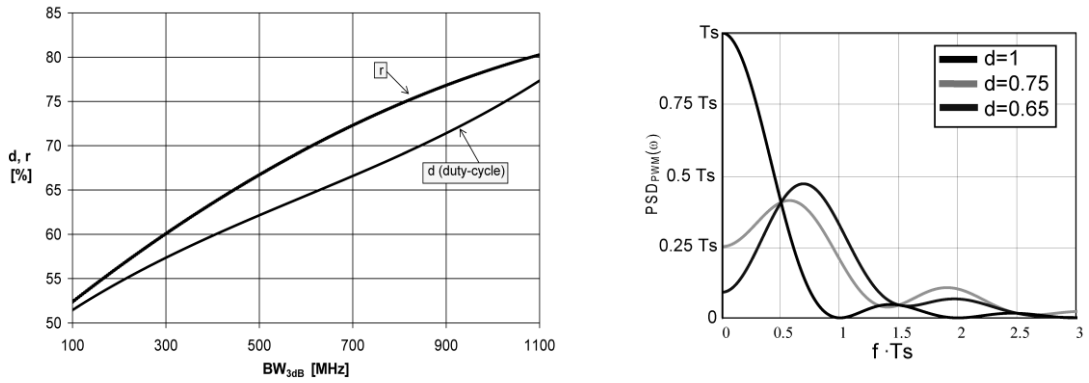
Fig. 2. a) PWM and FIR pulse definition, b) Channel impulse response analysis for both pre-emphasis methods (BW_{3dB} = 0.35 GHz).

Note that for optimal r, d parameter settings for each channel the channel output pulse becomes much narrower than the response to a plain NRZ pulse (r = 1, d = 100 %). This reduces the ISI contributions significantly. In Fig. 2b, the pulse definition to power spectral density calculations (PSD) for both methods is shown. By taking into account the Fourier transform of PWM pulse and using the formula for PSD of the stochastic signal [5] we get the expression for PSD_{PWM} as

$$PSD_{PWM}(\omega) = \frac{\left|P_{pwm}(\omega)\right|^2}{Ts} \sum_{k=-\infty}^{k=\infty} R(k) \cdot e^{j\omega kTs} = 2 \cdot \frac{3 - 2\cos(\omega(d-1)Ts - 2\cos(\omega dTs) + \cos(\omega Ts)}{\omega^2 Ts}, \quad (3)$$

where $P_{pw}(\omega)$ is the Fourier transform of $p_{pw}(t)$ and $R(k)$ *is* the autocorrelation function for a well known polar NRZ signaling (because $R(k)$ is the same for PWM as for polar NRZ) and is completely calculated in [5].

The function is graphically illustrated for three different *d* values of the PWM filter in Fig. 3b. It is obvious that the spectrum is shaped and moved to higher frequencies. The spectrum is more boosted at higher frequencies above the Nyquist frequency (0.5 on the axis) approximately for *d* values from 0.65 or less. The PSD function of conventional FIR filters is still decreasing until maximum pre-emphasis setting $r = 0.5$ without any spectrum boosting at the Nyquist frequency. It can be an important factor for the higher performance to compensate more lossy channels.



a) b)

Fig. 3. a) Relationship between BW_{3dB} and optimum coefficient settings, b) PSD Power spectral densities for the PWM pulse.

2.3. FREQUENCY DOMAIN COMPARISON

The theoretical channel and higher-order channel are used to calculate the equalized channel transfer function for the FIR filter and the PWM filter, see Fig. 1b. A bit length $T_S = 200$ ps corresponds with a bit period for the 5 Gbps data rate. The optimal values for the *r* parameter and *d* parameter are chosen for each channel setting to minimize an inter-symbol interference (ISI), see Fig. 2a. The decisive factor for the performance of the proposed equalizer is how the overall swing is reduced in order to achieve the reduction in a minimum-to-maximum loss for the system. This "flattening" of the magnitude of the frequency response analyzed in Fig. 4 is a good qualitative way to view the benefit of the equalization. Now the flatness in the frequency interval [0, f_N] is analyzed. The final results show that for theoretical 1st order channels both pre-emphasis methods are suitable to compensate channel losses which do not exceed 6 dB loss for maximum channel losses ($BW_{3dB} = 100$ MHz) after the equalization. Similarly, the equalized transfer function of channel with the higher-order transfer function (CH3) was performed. A significant difference between both pre-empasis methods can be seen if the higher-order channel is equalized. Fig. 4 shows the loss compensation of both pre-emphasis methods for optimal coefficient settings. In the case of PWMPE filter the total variation in the loss decreased from −6 dB to −20 dB for the optimal pre-emphasis setting ($d = 0.56$, $BW_{3dB} = 350$ MHz), see Fig. 4.

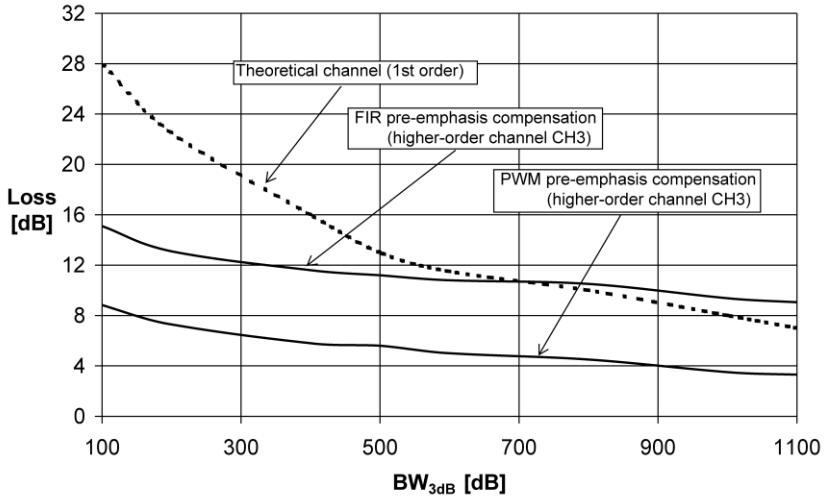


Fig. 4. The effect of loss compensation for both pre-emphasis techniques.

3. CONCLUSIONS

A perspective digital pre-emphasis technique based on the pulse-width modulation (PWM) is introduced. In the first part of the paper, the analyzed higher-order channel is described. The PWM method does not tune the pulse amplitude (as in the FIR pre-emphasis), but instead exploits the timing resolution. This fits well for today and the future low voltage high-speed CMOS processes. For the 1st order channels both pre-emphasis methods are similarly capable to compensate high channel losses. For a higher-order channel the situation is somewhat different. The reduction in the loss variation in our example (BW_{3dB} = 0.35 MHz) allows to shift the frequency at which the eye closes completely from 0.5 to 2.5 GHz for PWM filter. The reduction in the loss variation (note that our maximum loss is at the Nyquist frequeny 2.5 GHz) approximately only triples the frequency at which the eye closes completely from 0.5 to 1.5 GHz for the FIR filter. Another advantage is that the PWM pre-emphasis filter can be adjusted to the PCB backplane using only a single coefficient.

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REFERENCES

[1] Hall, S.H., Heck, H., *Advanced Signal Integrity for High-Speed Digital Design*. John Willey & Sons, New Yersey, 2009.

[2] Kollipara, R., Yeh, G.-J., Chia, B., Agarwal, A., "Design, Modeling and Characterization of High-Speed Backplane Interconnects," DesignCon 2003, Jan. 2003.

[3] Ševčík, B., "High-Speed Serial Differential Signaling Links with Commercial Equalizer," In *Proceedings of 20th International Conference Radioelektronika 2010*, 2010, Brno, pp. 191-194.

[4] Yang, C. K., Farjad, R., Horowitz, M., A 0.5-µm CMOS 4.0-Gbit/s Serial Link Transceiver With Data Recovery Using Over Sample Circuits, *IEEE Journal of Solid-State Circuit*, vol. 33, no. 5, May 1998, pp. 713-722.

[5] Couch, L.W., *Digital and Analog Communication Systems*, Prentice-Hall, New York, 2001.